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Question Paper Code : 86580

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Sixth Semester

Electronics and Communication Engineering

EC 1354 – VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulations 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Justify: CMOS is the best technology for analog and digital system.

2. Why are p-mos larger than n-mos in CMOS design?

3. Sketch the stick diagram for a tri-state buffer.

4. Draw the CMOS circuit for the following logic equation $f = \overline{a.b + c.d}$, using smallest number of transistor.

5. Write a short note on charge sharing.

6. Why parasitic delay calculation is important in CMOS circuits?

7. What are the different types of CMOS testing?

8. What is delay modeling?

9. List the various types of design styles in verilog HDL.

10. Write an expression to generate and propagate signals in a circuit using verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) Describe in detail about the different MOS models and explain about the small signal AC characteristics of MOS transistor. (16)

Or

(b) (i) Explain in detail about the body effect and its effect in NMOS and PMOS devices. (8)

(ii) Describe in detail about the various design issues in the logical and physical level of VLSI process. (8)

12. (a) Design a CMOS and Dynamic CMOS circuits that implements the function f = c.k.r + r.k.p + g.m. Assess the efficiency of each schemes and compare their performances. (16)

Or

(b) Design a 16:1 Multiplexer using

(i) CMOS and (8)

(ii) Transmission Gates assess the efficiency of each implementation. (8)

13. (a) (i) Explain in detail about the scaling concept and design margin concepts. (12)

(ii) Write short notes about the transistor sizing for the performance in combinational Networks. (4)

Or

(b) Describe in detail about the resistance and capacitance estimation calculation in a CMOS circuit with the proper loads and drivers. (16)

14. (a) Explain in detail about binary decoders and priority encoders. (16)

Or

(b) (i) Design a 4:1 MUX using transmission gates. (8)

(ii) Construct an 8 : 1 multiplexer using 4 : 1 and 2 : 1 MUX units. (8)

15. (a) (i) Design a 4-bit ripple carry adder using behavioral model and write the Verilog HDL code to realize the circuit function. (10)

(ii) Explain any five operators used in Verilog HDL with specific examples. (6)

Or

(b) (i) Design a priority encoder using structural model and write the Verilog HDL code to realize the circuit function. (10)

(ii) Write a verilog HDL code for 4 bit magnitude comparator. (6)

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